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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,434	08/07/2003	Jae-Yoon Sim	8947-000059/US	8523

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,434	SIM, JAE-YOON	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-8* is/are rejected.

7)☒ Claim(s) *2,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Kaneko (U.S. Patent No. 5,663,911).

Regarding claims 1,5,8 Kaneko discloses a semiconductor memory device (Figure 13) comprising:

a first memory block (Figure 13, left) and a second memory block (Figure 13, right) , each memory block including a bitline pair (Figure 13, BL, /BL);

a sense amplifier (Figure13, S/A) provided between the first memory block and the second memory block;

bitline isolation circuits (203, 204) for selectively connecting the first memory block and the second memory block to the sense amplifier in response to a first bitline isolation signal and a second bitline isolation signal (Column 8, lines 53-67);

bitline equalizing circuits (Figure 13, 205, 206) for providing bitline precharge voltage to the bitline pair in response to a first bitline equalizing signal and a second bitline equalizing signal (Column 9, lines 1-4); and

a bitline equalizing voltage generator (Figure 13, 19a,19b) for generating bitline equalizing voltage by utilizing a voltage of the bitline isolation signals (Column 9, lines 2-4).

Regarding claims 3-4, Kaneko discloses wherein the memory device further comprising a bitline equalizing signal generator (Figure 11, 19) and a second bitline equalizing generator for selectively generating the first bitline equalizing signal and the second bitline equalizing signal fed from the bitline equalizing voltage or the external voltage in response to a first memory block selection signal and a second memory block selection signal (Column 7, lines 20-27).

Regarding claims 6-7, Kaneko discloses wherein the bitline equalizing voltage generator comprising a word line drive signal generator (Figure 11, 111) for generating the word line drive signal having a boost voltage level in response to a word line drive

signal provided by a row decoder (Figure 11, 112); and a bitline equalizing voltage driver for serving the word line drive signal as the bitline equalizing voltage in response to a word line drive pulse signal which is generated in response to the bitline precharge and the word line address signal (Column 6, lines 56-63), and wherein the bitline equalizing voltage driver comprising: a first pmos transistor (Figure 1) , a gate thereof being supplied the word line drive pulse signal, a source thereof being supplied the word line drive signal, and a second pmos transistor (Figure 1), a gate thereof being supplied the bitline precharge voltage, a drain thereof being supplied the bitline equalizing voltage, a source thereof being connected to the drain of the first pmos transistor (Figures 1-3)

Allowable Subject Matter

6. Claims 2, 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2, 9-10 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Kaneko (U.S. Patent No. 5,663,911), and others, does not teach the claimed invention having a transfer circuit for providing a half level of the equalized bitline isolation signal as bitline equalizing voltage when the first bitline isolation signal and the second bitline isolation signal are deactivated as claim 2 discloses, and a voltage divider having a first to a third resistors connected in series and connecting

between external voltage and ground voltage and wherein the first resistor is connected to a transistor at its both ends and a gate of the transistor receives a first enable signal as claim 9 discloses, and a voltage down converter having a diode connected nmos transistor and a resistor which are serially connected between the bitline equalizing voltage and a ground as claim 10 discloses.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER